Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A method for fabricating a semiconductor device, the method comprising:

forming a gate on a device formation region of a semiconductor substrate, and forming source and drain regions in the device formation region of the semiconductor substrate adjacent respective sides of the gate, wherein the gate comprises a gate dielectric layer, a gate conductive layer and sidewall spacers located at respective sidewalls of the gate conductive layer;

sequentially forming a buffer layer and an etch stop layer over the source region, the drain region and the gate to obtain an intermediate structure;

forming a planarized first interlayer insulating film over a surface of the intermediate structure, wherein the first interlayer insulating film is a silicon oxide film formed by high-density plasma chemical vapor deposition;

dry etching the first interlayer insulating [[layer]] film until portions of the etch stop layer disposed over the source region, the drain region and the sidewall spacers [[is]] are exposed to form self-aligned contact holes in the first interlayer insulating film over the source region and the drain region, respectively;

wet etching the etch stop layer to remove the portions of the etch stop layer disposed over the source region, the drain region and the sidewall spacers; and

forming respective contact pads by filling the self-aligned contact holes with conductive polysilicon.

2. (Previously presented) The method of claim 1, wherein the gate further comprises a hard mask formed on a surface of the gate conductive layer.

3. (Previously presented) The method of claim 1, wherein the sidewall spacer and the etch stop layer are formed of silicon nitride by chemical vapor deposition.

4. (Canceled)

5. (Currently amended) The method of claim 1, further comprising:

following wet etching of the etch stop layer, wet etching the buffer layer to remove the buffer layer from the source region, the drain region and [[gate]] the sidewall spacers.

6. (Canceled)

7. (Canceled)

8. (Original) The method of claim 5, wherein the buffer layer is formed of silicon oxide by thermal oxidation.

9. (Original) The method of claim 8, wherein the buffer layer is formed of a mid-temperature oxide (MTO) by low pressure chemical vapor deposition.

10. (Original) The method of claim 1, wherein the etch stop layer is formed of silicon nitride by chemical vapor deposition.

11. (Canceled)

12. (Original) The method of claim 1, wherein the wet etching of the etch stop layer comprises:

removing oxide film remnants on the etch stop layer by wet etching by with an oxide etchant; and

removing the etch stop layer using an oxide etching solution or a nitride etching solution.

13. (Previously presented) The method of claim 12, wherein the oxide etching solution includes a concentration of diluted hydrofluoric acid (HF) ranging from about 0.01 wt% through 0.001 wt%.

14. (Original) The method of claim 12, wherein the nitride etching solution includes phosphoric acid H_3PO_4.

15. (Previously presented) The method of claim 14, wherein the concentration of phosphoric acid H_3PO_4 in the nitride etching solution ranges from about 50 wt% through 80 wt%.

16. (Previously presented) The method of claim 5, wherein the buffer layer is removed using an etching solution including ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and deionized water.

17. (Previously presented) The method of claim 16, wherein the etching solution includes a concentration of ammonium hydroxide (NH_4OH) ranging from about 0.1 wt% through 1.0 wt%.

18. (Previously presented) The method of claim 16, wherein the etching solution includes a concentration of hydrogen peroxide (H_2O_2) ranging from about 4.0 wt% through 7.0 wt%.

19. (Original) The method of claim 16, wherein the wet etching is performed at a temperature of 30°C through 80°C.

20. (Original) The method of claim 1, wherein the forming of the respective contact pads comprises:

filling the self-aligned contact holes by depositing the conductive polysilicon over an entirety of the surface of the semiconductor substrate; and

chemical mechanical polishing the conductive polysilicon in the self-aligned contact holes down to a level of an upper portion of the first interlayer insulating film.

21. (Currently amended) A method for fabricating a semiconductor device, the method comprising:

forming a gate on a device formation region of a semiconductor substrate, and forming source and drain regions in the device formation region of the semiconductor substrate adjacent respective sides of the gate, wherein the gate comprises a gate dielectric layer, a gate conductive layer and sidewall spacers located at respective sidewalls of the gate conductive layer;

forming a buffer layer over the source region, the drain region and the sidewall spacers of the gate;

forming an etch stop layer on the buffer layer to obtain an intermediate structure;

forming a first interlayer insulating film over the intermediate structure, wherein the first interlayer insulating film has an etching rate slower than the etching rate of the buffer layer relative to a defined dry etching process;

performing the dry etching process to etch the first interlayer insulating [[layer]] film until portions of the etch stop layer disposed over the source region, the drain region and the sidewall spacers [[is]] are exposed to form self-aligned contact holes in the first interlayer insulating film over the source region and the drain region, respectively;

wet etching the buffer layer and the etch stop layer to expose the source region, the drain region and the sidewall spacers; and

forming respective contact pads by filling the self-aligned contact holes with conductive polysilicon.